

a second gate-gate electrode layer including a gate electrode of a second load transistor and a gate electrode of a second driver transistor;

a first drain-drain wiring layer which forms a part of a connection layer that electrically connects a drain region of the first load transistor and a drain region of the first driver transistor;

a second drain-drain wiring layer which forms a part of a connection layer that electrically connects a drain region of the second load transistor and a drain region of the second driver transistor;

a first drain-gate wiring layer which forms a part of a connection layer that electrically connects the first gate-gate electrode layer and the second drain-drain wiring layer; and

a second drain-gate wiring layer which forms a part of a connection layer that electrically connects the second gate-gate electrode layer and the first drain-drain wiring layer,

wherein the first drain-gate wiring layer and the second drain-gate wiring layer are located in different layers, respectively, and

wherein a width of the first gate-gate electrode layer in the first load transistor is larger than the width of the first gate-gate electrode layer in the first driver transistor.

14. A memory system provided with the semiconductor device defined in claim 1.

15. An electronic apparatus provided with the semiconductor device defined in claim 1.

Please add the following new claims:

16. (Newly Added) A method for fabricating a semiconductor device comprising:

providing a first gate-gate electrode layer including a gate electrode of a first load transistor and a gate electrode of a first driver transistor;

providing a second gate-gate electrode layer including a gate electrode of a second load transistor and a gate electrode of a second driver transistor;

electrically connecting a drain region of the first load transistor and a drain region of the first driver transistor via a first drain-drain wiring layer which forms a part of a connection layer;

electrically connecting a drain region of the second load transistor and a drain region of the second driver transistor via a second drain-drain wiring layer which forms a part of a connection layer;

electrically connecting the first gate-gate electrode layer and the second drain-drain wiring layer via a first drain-gate wiring layer which forms a part of a connection layer;

electrically connecting the second gate-gate electrode layer and the first drain-drain wiring layer via a second drain-gate wiring layer which forms a part of a connection layer;

placing the first drain-gate wiring layer and the second drain-gate wiring layer in different layers, respectively; and

making a width of the first gate-gate electrode layer in the first load transistor larger than the width of the first gate-gate electrode layer in the first driver transistor.

17. (Newly Added) The method according to claim 16 further comprising making a width of the second gate-gate electrode layer in the second load transistor larger than the width of the second gate-gate electrode layer in the second driver transistor.

18. (Newly Added) The method according to claim 16 comprising:

providing a first adjacent memory cell which located adjacent to a side of the memory cell where the first gate-gate electrode layer is provided, wherein the first adjacent memory cell includes a third gate-gate electrode layer having a gate electrode of a third load transistor and a gate electrode of a third driver transistor;

using a first impurity layer as a source region by the first load transistor and the third load transistor;

providing a first contact section on the first impurity layer; and

providing the first contact section in a region other than a region between the first gate-gate electrode layer and the third gate-gate electrode layer.

19. (Newly Added) The method according to claim 16 further comprising:

locating a second adjacent memory cell adjacent to a side of the memory cell where the second gate-gate electrode layer is provided, wherein the second adjacent memory cell includes a fourth gate-gate electrode layer having a gate electrode of a fourth load transistor and a gate electrode of a fourth driver transistor;

using a second impurity layer as a source region by the second load transistor and the fourth load transistor;

providing a second contact section on the second impurity layer, and

providing the second contact section in a region other than a region between the second gate-gate electrode layer and the fourth gate-gate electrode.

20. (Newly Added) The method according to claim 16 further comprising:

electrically connecting the first drain-gate wiring layer to the second drain-drain wiring layer through a contact section; and

electrically connecting the second drain-gate wiring layer to the second gate-gate electrode layer through a contact section, electrically connected to the first drain-drain wiring layer through a contact section.

21. (Newly Added) The method according to claim 16 further comprising locating the first drain-gate wiring layer in a layer lower than the second drain-gate wiring layer.

22. (Newly Added) The method according to claim 16 further comprising locating the first drain-gate wiring layer in a layer in which the first gate-gate electrode layer is provided.

23. (Newly Added) The method according to claim 16 further comprising forming the second drain-gate wiring layer across a plurality of layers.